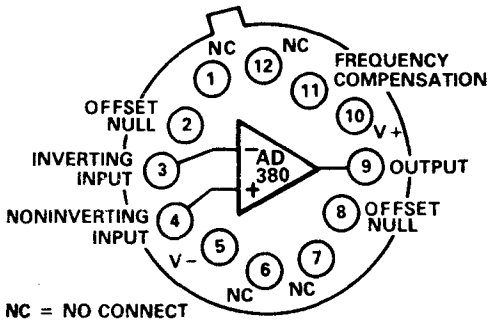
Wideband, Fast-Settling FET-Input Op Amp

AD380

FEATURES
High Output Current: 50mA @ ±10V
Fast Settling to 0.1%: 130ns
High Slew Rate: 330V/μs
High Gain-Bandwidth Product: 300MHz
High Unity Gain Bandwidth: 40MHz
Low Offset Voltage (1mV for AD380K, L, S)

AD380 FUNCTIONAL BLOCK DIAGRAM



TOP VIEW

PRODUCT DESCRIPTION

The AD380 is a hybrid operational amplifier that combines the low input bias current advantages of a FET input stage with the high slew rate and line driving capability of a fast, high power output amplifier.

The AD380 has a slew rate of 330V/μs and will output ±10V at ±50mA. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate, or settling time for the given application.

A true differential input ensures equally superior performance in all system designs whether they are inverting, noninverting, or differential.

The AD380 is especially designed for use in applications, such as fast A/D, D/A and sampling circuits, that require fast and smooth settling and FET input parameters.

The AD380 is offered in three commercial versions, J, K and L specified from 0 to +70°C and one extended temperature version, the S, specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-8 style cans.

PRODUCT HIGHLIGHTS

1. The AD380's high output current (50mA @ ±10V) makes it suitable for driving terminated 200Ω twisted pairs.
2. The fast settling output (250ns to 0.01%) makes the AD380 an ideal choice for video A/D and D/A converters and sample and hold applications.
3. The settling wave forms are not only fast but are also very smooth. The absence of large overshoot and oscillations makes the AD380 a very predictable and dependable system element.
4. The high gain-bandwidth product (300MHz) ensures low distortion in high frequency applications.
5. Quick, symmetrical overdrive recovery time (250ns) is assured by an internal antisaturation diode. This is useful in applications where large transient signals may occur.
6. The precision input (1mV offset, max), along with fast settling and high current output make the AD380 an excellent choice for:
   - ATE pin drivers
   - precision coax buffers
   - signal conditioning on pulse waveforms
   - high resolution graphics displays.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD380JH	AD380KH	AD380LH	AD380SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, no load	40,000 min	*	*	*
V_{OUT} = ±10V, $R_L \geq 200\Omega$	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 200Ω, T_A = min to max	±12V (±10V min)	*	*	*
Output Impedance (Open Loop)	100Ω	*	*	*
Short Circuit Current	100mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	40MHz	*	*	*
Gain-Bandwidth Product, f = 100kHz, C_C = 1pF	300MHz (200MHz min)	*	*	*
Full Power Response	6MHz	*	*	*
Slew Rate, C_C = 1pF, 20V Swing	330V/μs (200V/μs min)	*	*	*
Settling Time: 10V Step to 1%	90ns	*	*	*
10V Step to 0.1%	130ns	*	*	*
10V Step to 0.01%	250ns	250ns (400ns max)	**	**
INPUT OFFSET VOLTAGE	2.0mV max	1.0mV max	**	**
vs. Temperature[1], T_A = min to max	50μV/°C max	20μV/°C max	10μV/°C max	50μV/°C max
vs. Supply	1mV/V max	*	*	*
INPUT BIAS CURRENT				
Either Input, Initial[2]	10pA (100pA max)	*	*	*
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{11}\Omega \| 6pF$	*	*	*
Common Mode	$10^{11}\Omega \| 6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[3]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	60dB min	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(6 to 20)V	*	*	*
Quiescent Current	12mA (15mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz to 100Hz	3.3μV p-p (0.5μV rms)	*	*	*
100Hz to 10kHz	6.6μV p-p (1μV rms)	*	*	*
10kHz to 1MHz	40μV p-p (6μV rms)	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance θ_{JA}	100°C/W	*	*	*
θ_{JC}	70°C/W	*	*	*
PACKAGE OPTION[4]				
TO-8 Style	H-12A	*	*	*

NOTES

[1]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of offset nulled.

[2]Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures see Figure 16.

[3]Defined as the maximum safe voltage between inputs such that neither exceeds ±10V from ground.

[4]See Section 20 for package outline information.

*Specifications same as AD380JH.

**Specifications same as AD380KH.

Specifications subject to change without notice.

Typical Characteristics – AD380

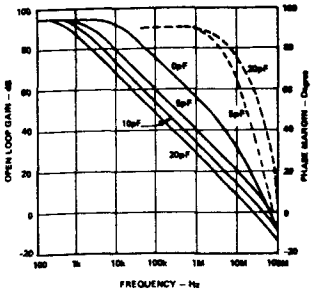


Figure 1. Open Loop Frequency Response

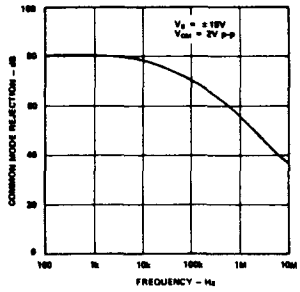


Figure 2. CMRR vs. Frequency

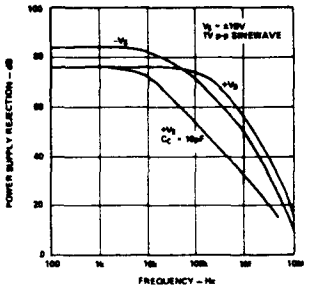


Figure 3. PSRR vs. Frequency

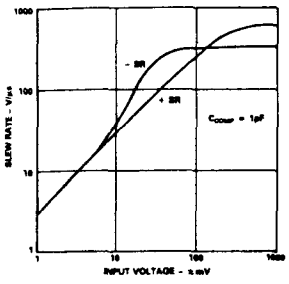


Figure 4. Slew Rate vs. Differential Input Voltage

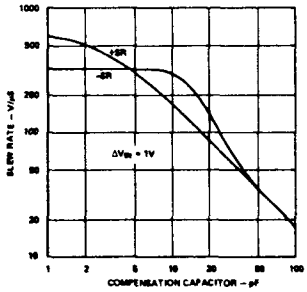


Figure 5. Slew Rate vs. Compensation Capacitor

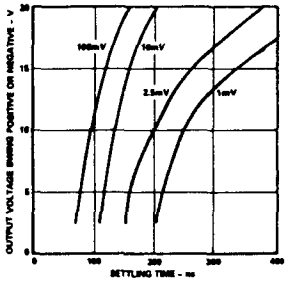


Figure 6. Output Settling Time vs. Output Voltage Swing and Error

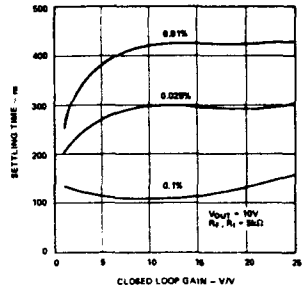


Figure 7. Settling Time vs. Closed Loop Gain

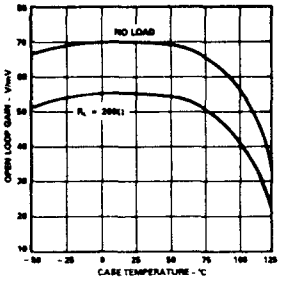


Figure 8. Gain vs. Temperature

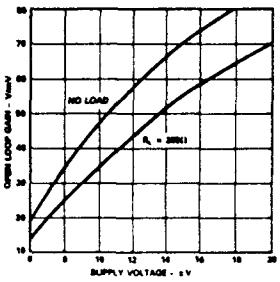


Figure 9. Gain vs. Supply Voltage

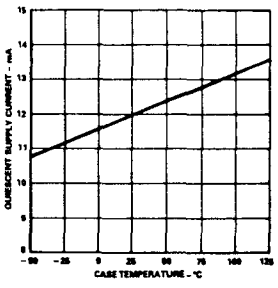


Figure 10. Supply Current vs. Temperature

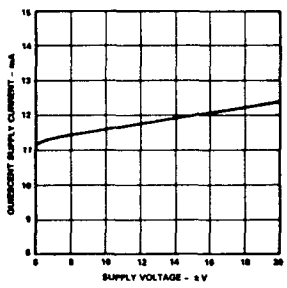


Figure 11. Supply Current vs. Supply Voltage

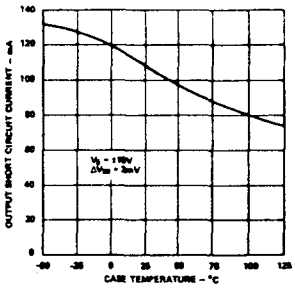


Figure 12. I_{SC} vs. Temperature

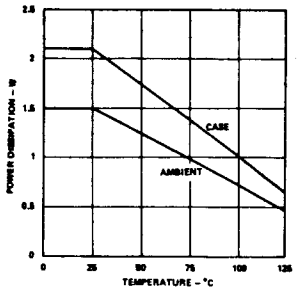


Figure 13. Power Dissipation vs. Temperature

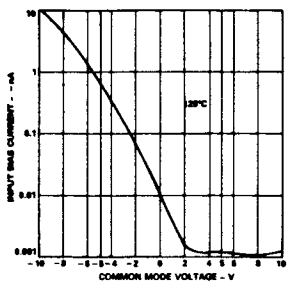


Figure 14. Input Bias Current vs. Common Mode Voltage

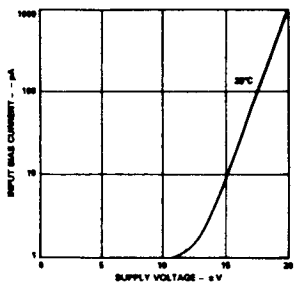


Figure 15. Input Bias Current vs. Supply Voltage

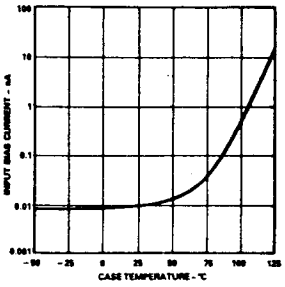


Figure 16. Input Bias Current vs. Temperature

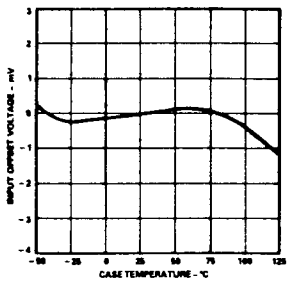


Figure 17. Offset Voltage vs. Temperature

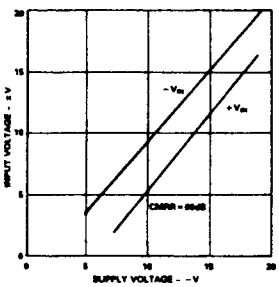


Figure 18. Input Voltage Range vs. Supply Voltage

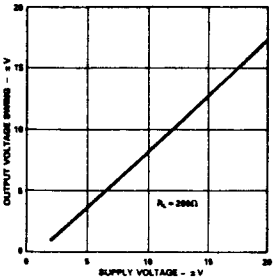


Figure 19. Output Voltage Swing vs. Supply Voltage

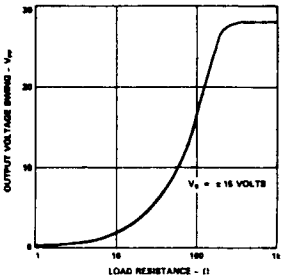


Figure 20. Output Voltage Swing vs. Load Resistance

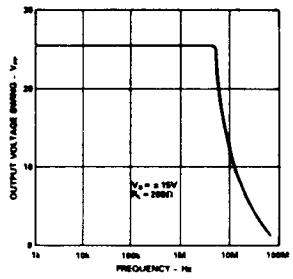


Figure 21. Large Signal Frequency Response

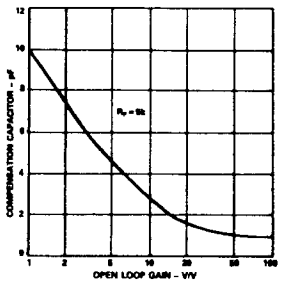


Figure 22. Recommended Compensation Capacitor vs. Closed Loop Gain

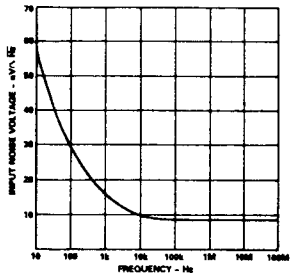


Figure 23. Input Noise Voltage Spectral Density

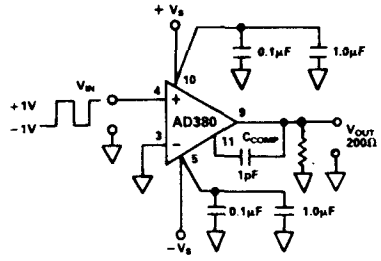


Figure 24a. Overdrive Recovery Test Circuit

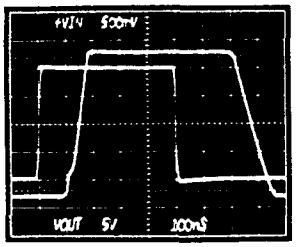


Figure 24b. Overdrive Recovery Response (Symmetrial 20ns Version Available)

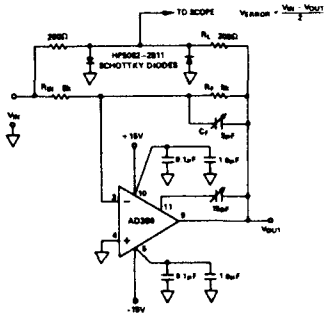


Figure 25a. Unity Gain Inverter Settling Time Test Circuit

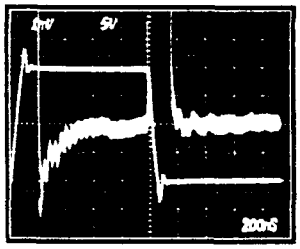


Figure 25b. Unity Gain Inverter Large Signal Response

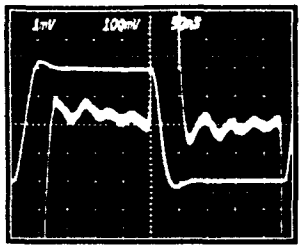


Figure 25c. Unity Gain Inverter Small Signal Response

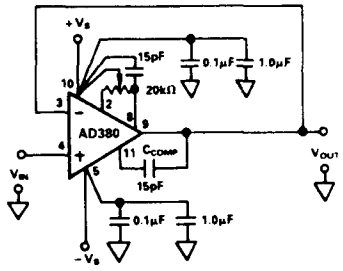


Figure 26a. Unity Gain Buffer Circuit

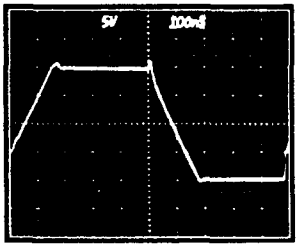


Figure 26b. Unity Gain Buffer Large Signal Response

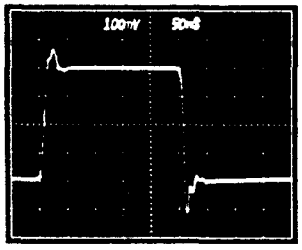


Figure 26c. Unity Gain Small Signal Response

APPLICATIONS INFORMATION

Compensation Capacitor

For low gain applications a 5pF to 27pF capacitor between the frequency compensation input (pin 11) and the output (pin 9) will reduce the risk of oscillation by adding phase margin. A compensation capacitor is especially needed when driving capacitive loads. For gains greater than 30 a 1pF compensation capacitor is recommended; see Figure 22.

For unity gain buffer applications it may be necessary to add a small (10pF to 20pF) capacitor between pins 8 and 10 for improved phase margin; see Figure 26a.

Offset Null

If the initial offset voltage is not low enough for the user's application offset nulling is required. To null the offset tie a 20kΩ potentiometer between the offset null pins (pins 2 and 8). The wiper of the potentiometer is tied to the positive supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

To minimize the effects of offset voltage drift as a function of temperature, null the offset at the midpoint of the operating temperature range. For example, if the operating environment is 0°C to 70°C do the offset nulling at 35°C. This will insure a maximum offset voltage drift of 35 times the V_{OS} drift specification at either temperature extreme.

Typical Circuits

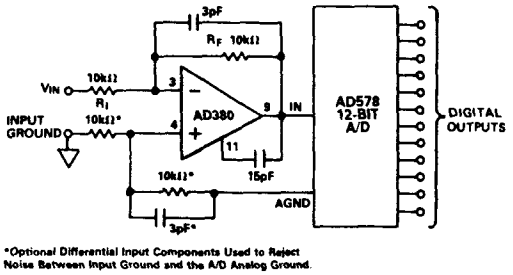


Figure 27. Fast-Settling Buffer

Its quick recovery from load variations makes the AD380 an excellent buffer for fast successive approximation A/D converters; see Figure 27.

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

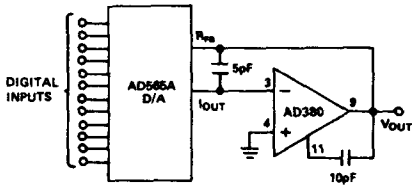


Figure 28. 12-Bit Voltage Output DAC Circuit Settles to 1/2LSB in 300ns

The AD565A 12-bit digital to analog converter with an AD380 output amplifier will give a voltage output that typically settles to within 1/2LSB in less than 300ns. Total settling time is the root mean square of the DAC current output settling time and the output amplifier settling time.

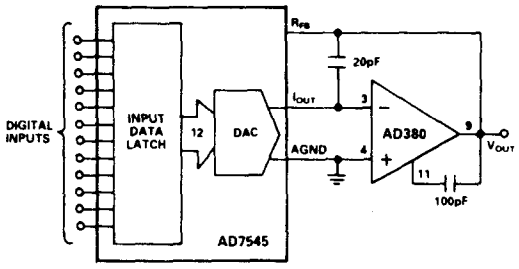


Figure 29. CMOS DAC Output Amplifier

CMOS DAC output amplifiers require low offset voltage op amps. The output impedance of CMOS DACs varies with input code. This can cause a code dependent error term at the output that approaches the op amps' offset voltage. If the DAC has a differential nonlinearity of 1/2LSB, it will require an output amplifier with less than 1/2LSB offset error to remain monotonic. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus, the AD380KH, with only 1mV offset maximum, will contribute less than 1/2LSB to differential linearity error.

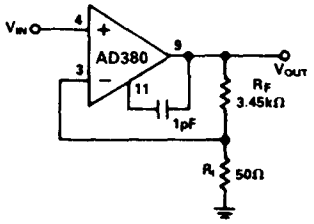


Figure 30. Video Amplifier

The high output current capability of the AD380 makes it suitable for video speed driver applications. In the circuit above the closed loop gain of 70 (37dB) is available over a bandwidth of 5MHz. Note that a 1pF compensation capacitor is required in this high gain application.